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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,902	03/11/2004	Sam Gat-Shang Chu	AUS920031079US1	7019

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

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06/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/798,902	CHU ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,8-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,8-16,18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 04/30/2007 has been entered.

2. Claims 4-6,8-16,18-20 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 4-6,8-16,18-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 4, 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Ho (U.S. Patent No. 5,629901).

Regarding claim 4, Ho discloses a register file (Figure 4) comprising:

a plurality of register file cells (Figure 4, 24) coupled to a bit line (Figure 4, BL);

a latch coupled to the bit line (Figure 4, 21,22); and

an inverter (Figure 5, 44) coupled between an output of the latch and the bit line (Figure 5, LCB) ;

wherein the inverter is a tri-state inverter (Figure 5, 44, Column 5, lines 34-35) receiving a hold select signal (Figure 5, sgb) to control operation of the inverter (Column 3, lines 35-49).

Regarding claim 11, Ho disclose a register file (Figure 4) comprising: a plurality of register file cells (Figure 4, 24) coupled to a bit line (Figure 4, BL); a latch (Figure 4, 21, 22) coupled to the bit line; and a transmission gate circuit (Figure 4, 31) coupled between an output of the latch and the bit line.

Regarding claim12, Ho discloses an inverter (Figures 8, 10) coupled between the bit line and an input of the latch, and wherein the output of the latch is an output of the register file (Figure 10).

6. Claims 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al. (U.S. Patent No. 5,590,087).

Regarding claim 4, Chung et al. disclose a register file (Figure 1, 1) comprising:

a plurality of register file cells (Figure 1) coupled to a bit line (Column 1, lines 45-50);

a latch coupled to the bit line (2E, 520, 521); and

an inverter (Figure 2A, 106) coupled between an output of the latch and the bit line (Column 2, lines 60-65) ;

wherein the inverter is a tri-state inverter (Column 3, lines 14-20) receiving a hold select signal (Column 3, lines 14-20) to control operation of the inverter.

Regarding claim 5, Chung et al. disclose wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch (Figures 2E, 3, 40, 44, 46).

Regarding claim 6, Chung et al. disclose wherein data is read out of the register array to be input into the latch (Figure 2E, 523).

7. Claim 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Raje (U.S. Patent No. 6,195,123).

Regarding claim 4, Raje disclose a register file (ABSTRACT) comprising:

a plurality of register file cells (Figure 1, 10, Figure 2, 18) coupled to a bit line (Figure 2, BITLINE);

a latch coupled to the bit line (Figure 2, Z); and

an inverter (Figure 2) coupled between an output of the latch and the bit line (Figure 2) ;

wherein the inverter is a tri-state inverter (Figure 5, 106) receiving a hold select signal (92) to control operation of the inverter.

Regarding claim 5, Raje discloses wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch (Figure2, CLK, inveter and transistors).

Regarding claim 6, Raje discloses wherein data is read out of the register array to be input into the latch (Figure 2).

Regarding claims 8, 10, Raje discloses a register file (Figure 4) comprising:

a first plurality of cells (Figure 4, 50) coupled to a first local bit line (Figure 4, LOCAL BIT LINE);

a global bit line (Figure 4, GLOBAL BIT LINE);

a first-state inverter (Figure 5, 106) coupled between the first local bit line and the global bit line (Figures 4-5), the first Iri-state inverter controlled by a first local select signal (Figure 5, 92);

a second plurality of cells (Figure 4, 60) coupled to a second local bit line (Figure 4);

a second tri-state inverter (Figure 4, 64, Figure 5, 64 and 116) coupled between the second local bit line and the global bit line (Figure 5), the second tri-state inverter controlled by a second local select signal (Figure 5, 92);

a latch with its input coupled to the global bit line (Figure 5, 104) ; and

a third tri-state inverter (Figure 4, 64) coupled between an output of the latch and the global bit line, the third tri-state inverter controlled by a hold signal (92).

Regarding claim 9, Raje discloses an inverter (Figure 1) coupled between the global bit line and the input of the latch.

Regarding claims 11, 18 , Raje discloses a register file (Figure 1) comprising: a plurality of register file cells (Figure 2, 18) coupled to a bit line (Figure2, BITLINE);

a latch (Figure 2, Z) coupled to the bit line; and

a transmission gate circuit (Figure 2, CLK, inverter, transistors) coupled between an output of the latch and the bit (Figure 2).

Regarding claims 12-16, 19-20, Raje discloses an inverter coupled between the bit line and an input of the latch (Figure 2), and wherein the output of the latch is an output of the register file (Figure 5), and wherein the transmission gate circuit receives a hold select signal (Figure 5, 92), and wherein an output of the transmission gate circuit is coupled to the bit line and wherein an input of the transmission gate circuit is coupled to the output of the latch (Figure 2), and wherein data is read out of the register array to be input into the latch (Figure 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827